Analysis of CMOS Interconnections Combining LE-FDTD Method and SOC Procedure

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Abstract— **This work describes the application of the Lumped Element-Finite Difference Time Domain (LE-FDTD) method to the rigorous analysis of CMOS interconnections. In particular the frequency-dependent line parameters are evaluated in a wide (DC to 100 GHz) bandwidth. To obtain very accurate results the Short-Open Calibration (SOC) procedure has been adopted. With such an approach, simple lumped generators and loads can be used to excite and terminate the structure under analysis, in substitution of more complex boundary conditions. The technique has been validated against experimental results from the literature showing a good agreement.**

Index Terms: **CMOS interconnections, MIS transmission lines, numerical calibration, FDTD method.**

I. Introduction

CMOS interconnections and, more in general, transmission lines on semiconductor materials have been considered by many authors [1], [2], [3] showing the existence of two regions of operation: namely the slow-wave region and the dielectric quasi-TEM region. Because of complicate propagation mechanisms, the wide-band analysis of these structures is a challenging task: numerical simulators are usually adopted for the rigorous solution of the electromagnetic problem. Moreover a very high accuracy is required since, for example, the frequency-dependent line parameters are particularly sensitive to numerical errors in the computation of both characteristic impedance and propagation constant.

This paper proposes a combination between the Short-Open Calibration (SOC) procedure [4], and the Lumped Element-Finite Difference Time Domain (LE-FDTD) method [5]. With such an approach the interconnection experimented in [6], realized using a 0.25 μm CMOS technology, has accurately been characterized, accounting for the finite conductivity of the metal line as well as for the losses of the doped silicon substrate. Although the FDTD method was applied to the analysis of Metal-Insulator-Semiconductor (MIS) structures in [7], the proposed technique is numerically more efficient.

II. Method

The basic idea consists of using very simple lumped generators and loads, in substitution of more complex boundary conditions such as [8], [9], to provide a suitable excitation and termination to the structure under analysis. From the evaluation of the equivalent port voltages and currents a network representation of such a structure can be derived.

Unfortunately, experiments previously carried out by the authors, have demonstrated that the accuracy achievable with this approach is very poor. This is mainly due to the unavoidable, numerical discontinuities associated to the junction between lumped elements (generator or load) and distributed circuit. If, for example, an interconnection line is terminated with a lumped resistor, a step-like discontinuity is formed at the connecting point. Another source of systematic errors is the mesh-dependent parasitic capacitance in parallel with the lumped element [10].

A way to circumvent such a problem consist of representing these port discontinuities with an error network superimposed to the circuit being analyzed. With the SOC procedure, recently introduced in [4] and [11], this error network can be determined and thus de-embedded from that of the whole simulated structure. As a result, the equivalent network parameters of the distributed circuit can be computed very accurately, still using simple lumped excitation and termination schemes.

The equivalent network representation adopted to describe the CMOS interconnection is based on the transmission matrix. Using such a matrix, the output voltage and current (V_2, I_2) can be computed in terms of the input voltage and current (V_1, I_1) as follows:

$$\begin{aligned} V_2 &= \cosh(\gamma l)\, V_1 - Z_0 \sinh(\gamma l)\, I_1 \\ I_2 &= -\frac{\sinh(\gamma l)}{Z_0} V_1 + \cosh(\gamma l)\, I_1 \end{aligned} \qquad (1)$$

In the above system of equations, voltage and current at each reference plane of the structure have been determined combining the LE-FDTD method with the SOC procedure. After simple manipulations of (1) one obtains:

$$Z_0 = \sqrt{\frac{V_2^2 - V_1^2}{I_2^2 - I_1^2}} \tag{2}$$

$$\gamma = \frac{1}{l} \operatorname{acosh}\left[\frac{V_1 I_1 + V_2 I_2}{V_1 I_2 + V_2 I_1}\right] \tag{3}$$

and thus the characteristic impedance and the propagation constant (of the line equivalent to the CMOS interconnection) can be computed. Since the LE-FDTD simulator evaluates all the necessary electrical variables in the time domain, to apply the SOC technique and to extract the line parameters, the electrical variables must be converted into the frequency domain using a DFT algorithm.

III. Validation of the Method

To validate the proposed approach, the CMOS interconnection experimented in [6] has been considered. The transmission line is fabricated in the second metal level and features a thickness of $0.7\,\mu$m and a width of $1\,\mu$m. The conductivity of the silicon substrate is $\sigma_{Si} = 10^4\,$S/m. The other dimensions of the cross-section are reported in the caption of Fig. 1. These values, not available in [6], have been extrapolated from a standard $0.35\,\mu$m CMOS technology. The ground lines are connected directly to the conductive Si substrate by a continuous grid of stacked vias. In this work these lateral ground lines have been approximated by means of perfectly conducting walls while the open boundary on top is represented using an ideal magnetic boundary.

The interconnection has first been simulated with the LE-FDTD method; then the SOC procedure has been applied and both the characteristic impedance Z_0 and the propagation constant γ have been computed. Fig. 2 shows a comparison between these results and the measurements reported in [6]: the agreement is good although the critical dimensions of the cross-section have been extrapolated from a different CMOS technology.

The spatial resolution of the FDTD mesh is $\Delta x_{min} = 0.175\,\mu$m, $\Delta y_{min} = 0.125\,\mu$m and $\Delta z_{min} = 25\,\mu$m. The time discretization is taken to be $\Delta t = 0.5\,$fs. The computational volume is composed by $N_x \times N_y \times N_z = 40 \times 31 \times 55$ cells. The CPU time is about 200 minutes on a 650 MHz Pentium III laptop computer.

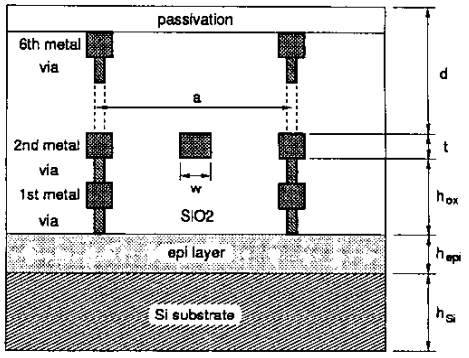

Fig. 1. Cross-section of the reference CMOS interconnection (not to scale). The dimensions are: $a = 130\,\mu$m; $w = 1\,\mu$m; $h_{Si} = 508\,\mu$m; $h_{epi} = 4.2\,\mu$m; $h_{ox} = 2.9\,\mu$m; $t = 0.7\,\mu$m and $d = 8.6\,\mu$m. The material parameters are: $\epsilon_{Si} = 11.7$; $\sigma_{Si} = 10^4\,$S/m; $\epsilon_{epi} = 11.7$; $\sigma_{epi} = 10\,$S/m; $\epsilon_{ox} = 3.9$ and $\sigma_{Al} = 27.8 \times 10^6\,$S/m.

Having determined Z_0 and γ, the frequency-dependent parameters are readily obtained from:

$$\begin{aligned} R + j\omega L &= \gamma Z_0 \\ G + j\omega C &= \gamma / Z_0 \end{aligned} \tag{4}$$

As an example, Fig. 3 illustrates the specific resistance and conductance. In the same figure, the results obtained without the SOC calibration, have also been depicted. The latter curves are affected by a large amount ripple that cannot be justified considering the behaviour of Z_0 and γ. Combining FDTD and SOC procedures this effect can be removed over a wide bandwidth, thus improving the accuracy of the results.

IV. Conclusions

The LE-FDTD method can successfully be combined with the SOC numerical calibration procedure in order to characterize integrated transmission lines. Experimental results from the literature, about a typical $0.25\,\mu$m CMOS interconnection, have been used to validate the approach. With respect to previous FDTD works, the proposed technique is numerically more efficient allowing a good accuracy to be obtained in a wide (DC to 100 GHz) frequency range.

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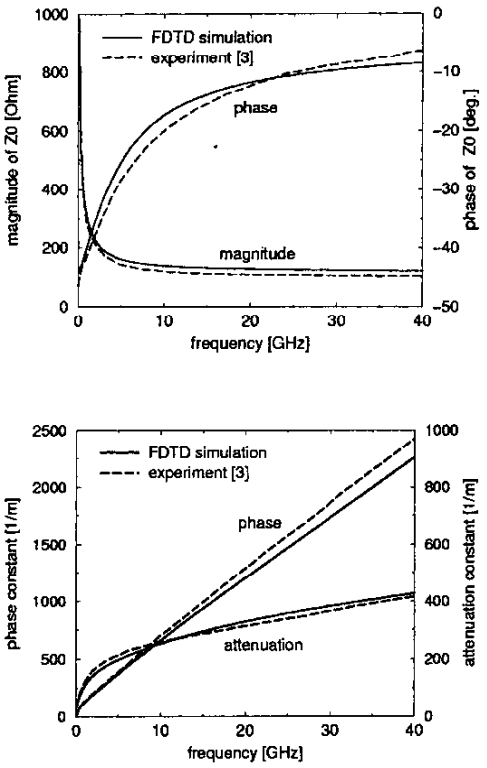

Fig. 2. Characteristic impedance (top) and propagation constant (bottom) of the reference CMOS interconnection: comparison with the experiment of Arz *et al.*

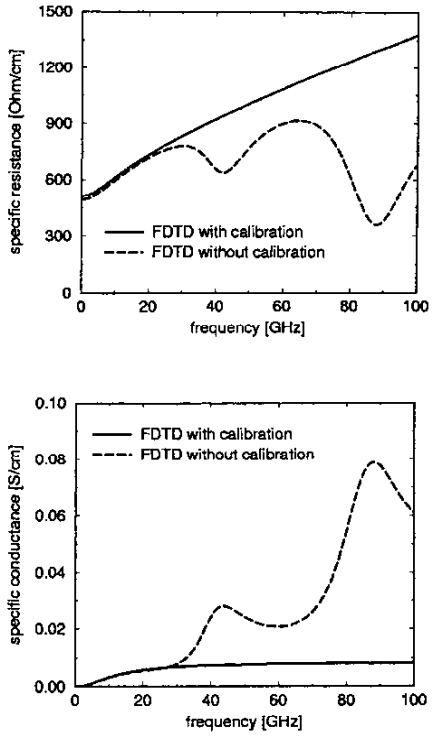

Fig. 3. Specific resistance (top) and conductance (bottom) of the reference CMOS interconnection. Without the SOC calibration procedure the curves are disturbed by a large amount of numerical ripple.

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